

EUVL Challenges for Next Generation Devices

Center for Semiconductor Research & Development

Advanced Lithography Process Technology Dept.

Tatsuhiko Higashiki

Contents

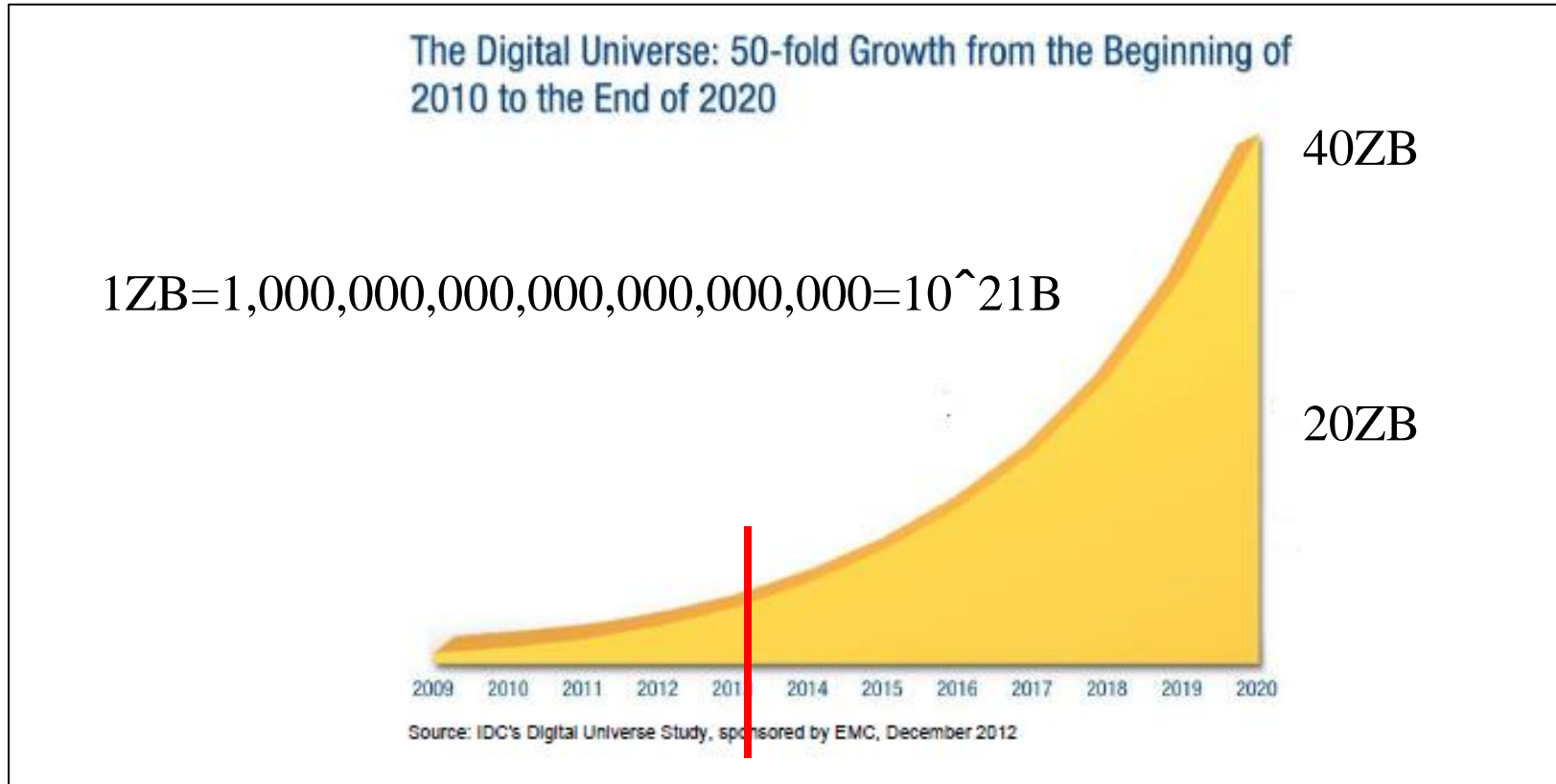
- **Device Roadmap and Lithography**
- **Extendibility toward 1x nm hp and beyond with New Lithography**
 - ✓ SAxP
 - ✓ EUVL
 - ✓ EUVL+DSA
- **Conclusion**

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Rapid Increase of Information Volume Demand

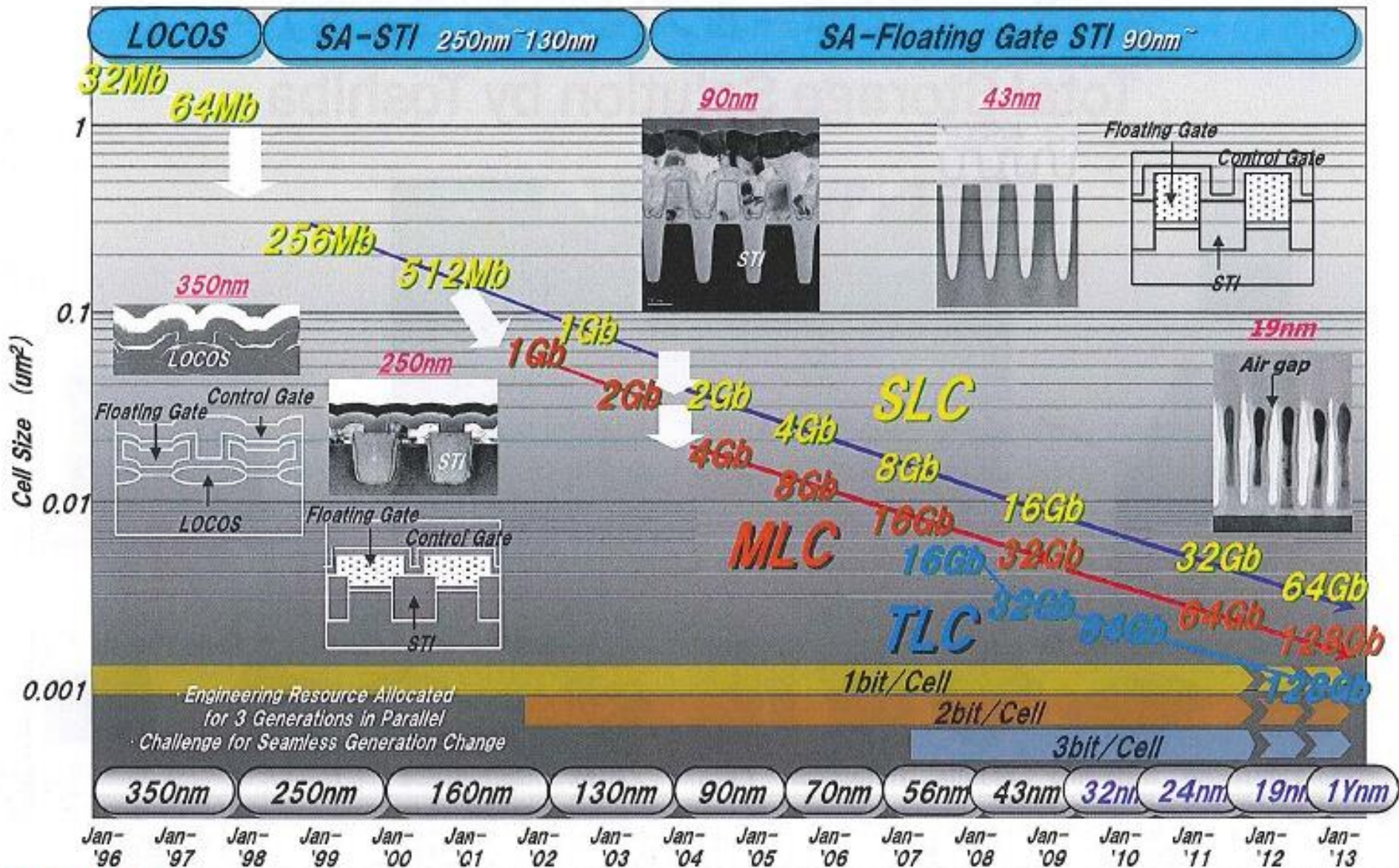
All information that is created, captured, replicated and/or consumed by all human on the planet.



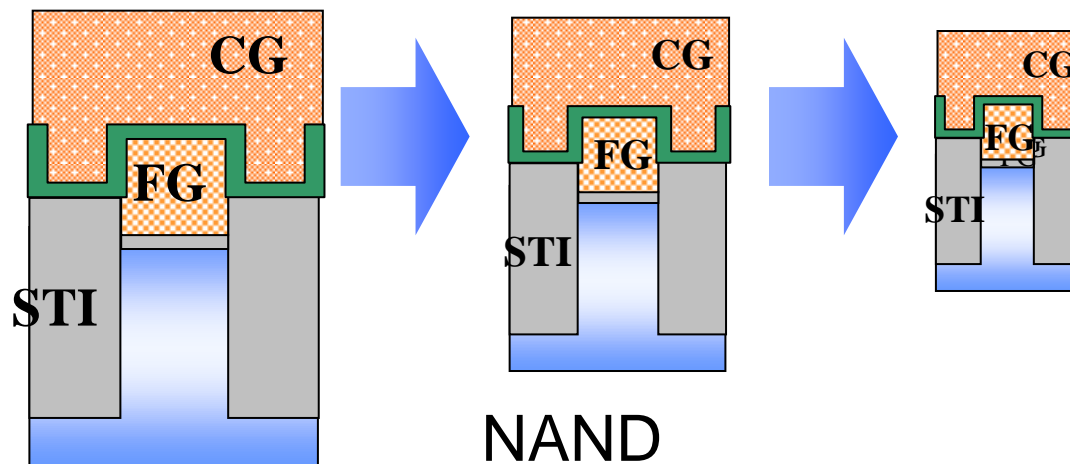
All information is not fully stored, but partially stored.

⇒ Need for larger-capacity memory in the future.

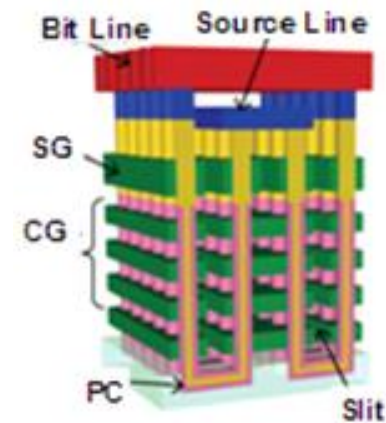
NAND Flash Memory Technology Roadmap



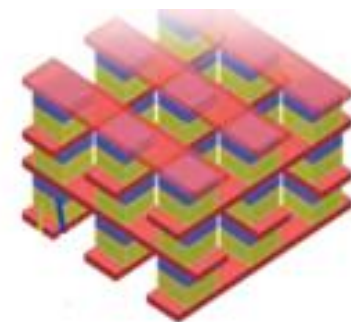
Roadmap of the Memory



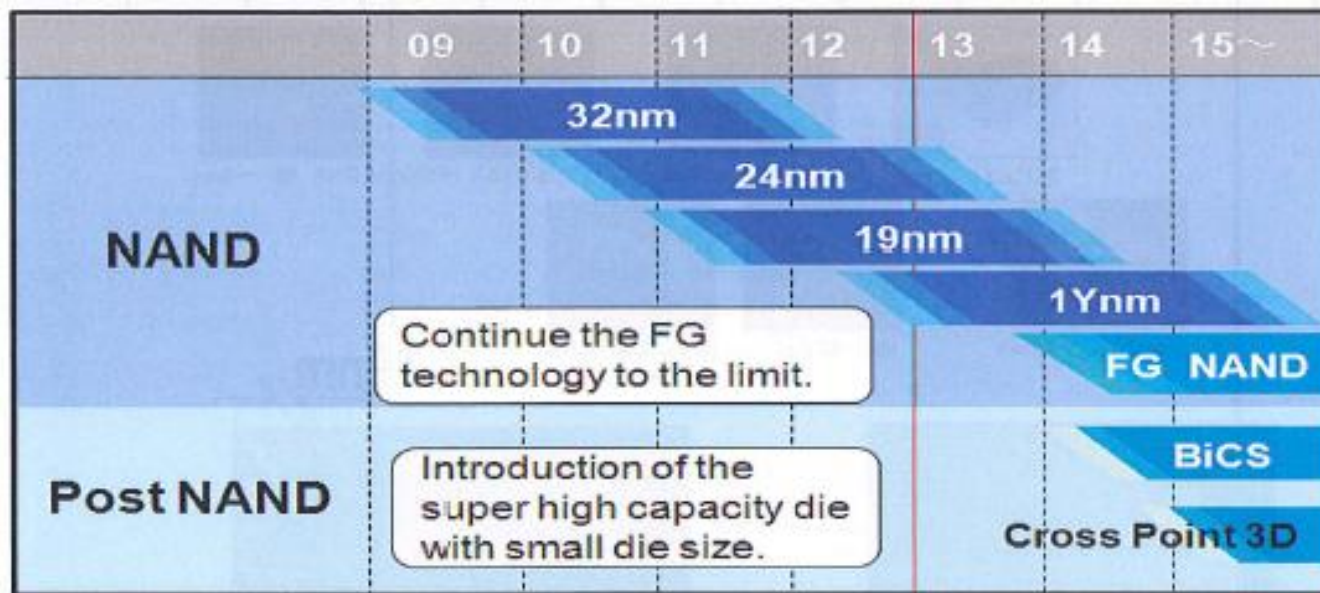
NAND



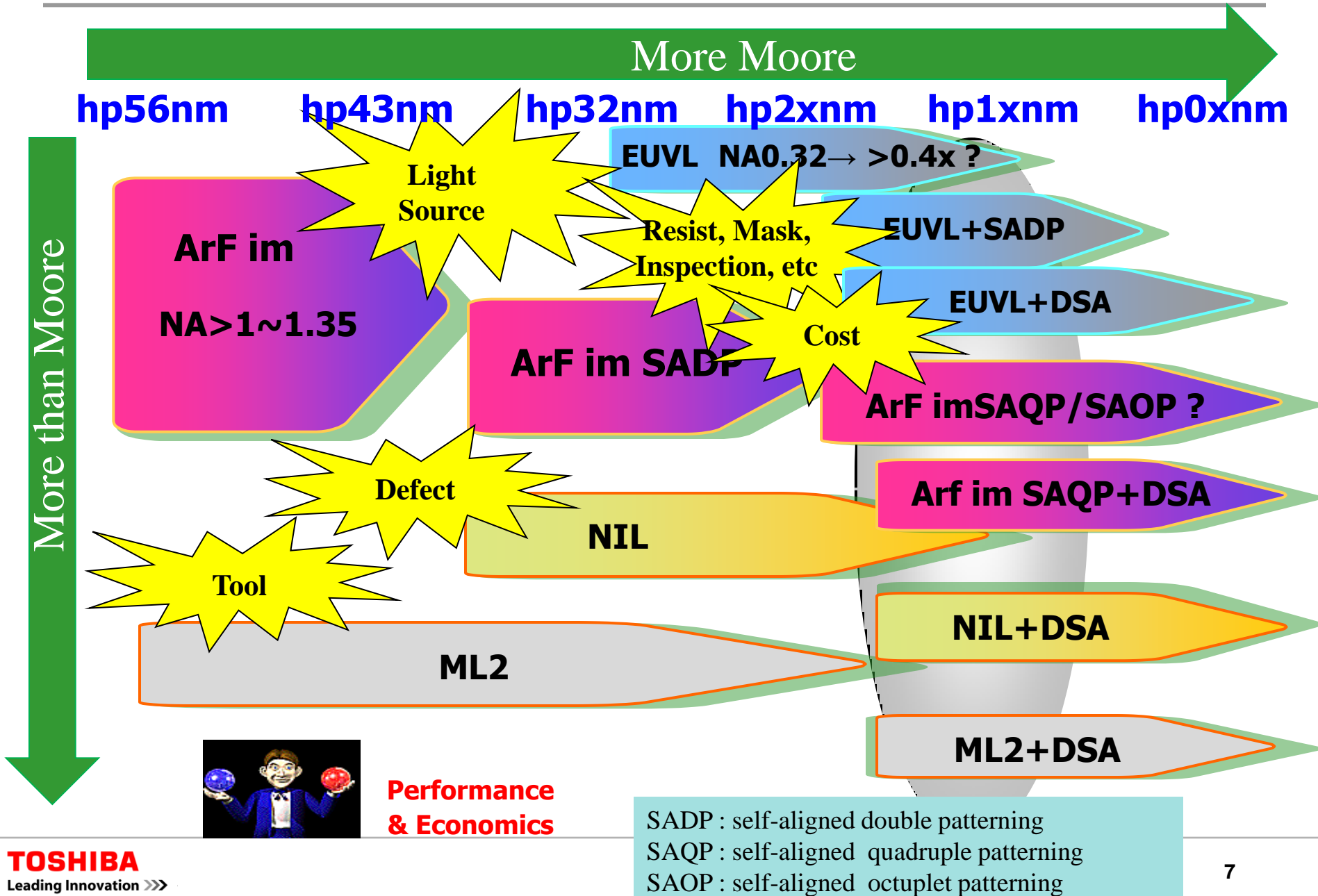
BiCS



Cross Point



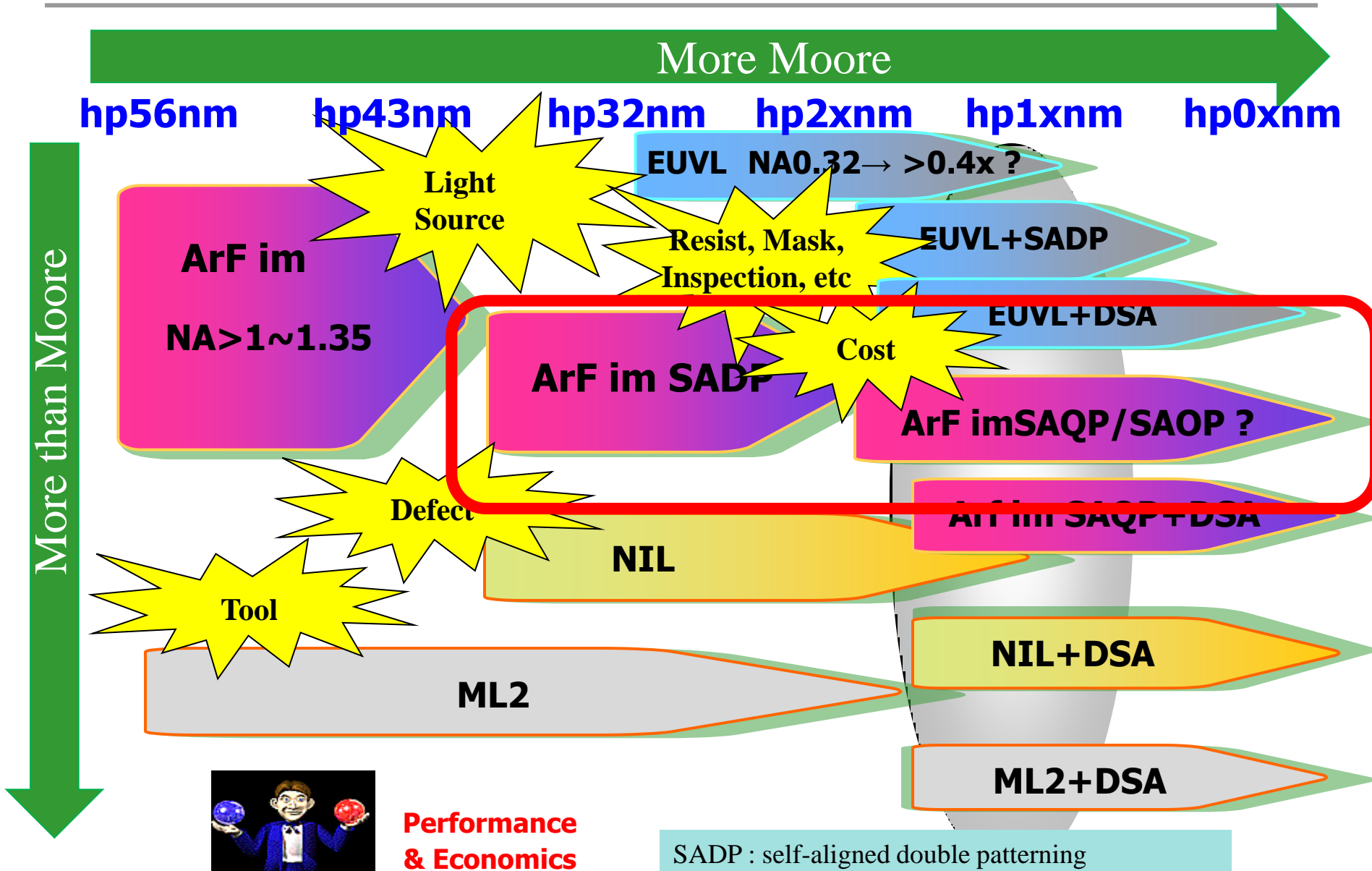
Lithography Challenges



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Lithography Challenges



**Performance
& Economics**

SADP : self-aligned double patterning
 SAQP : self-aligned quadruple patterning
 SAOP : self-aligned octuplet patterning

Single Exposure by Mask Technology Revolution

SADP

single

**Mask
(Template)**

Exposed

Processed

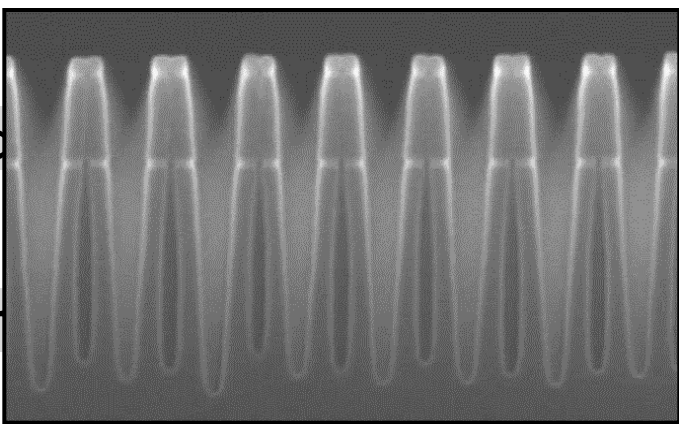
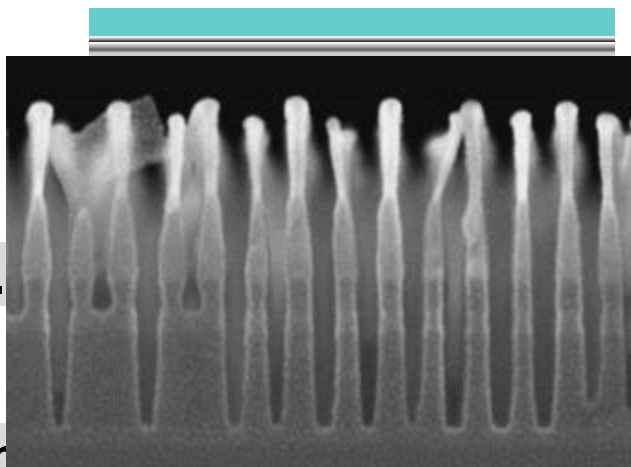
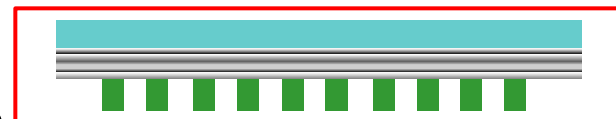
Litho.

Slimming

Film d

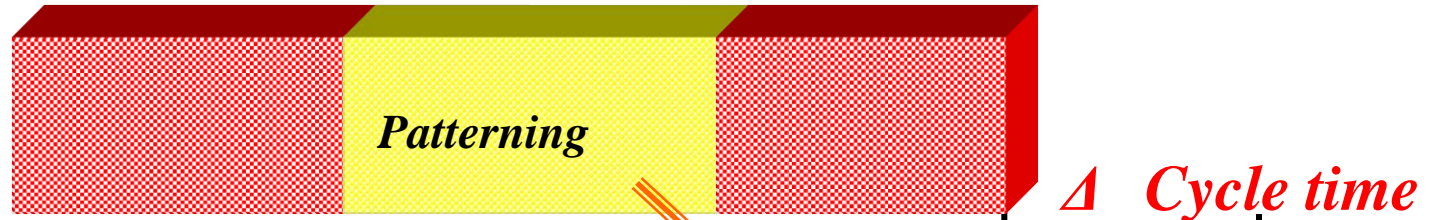
etching

etching

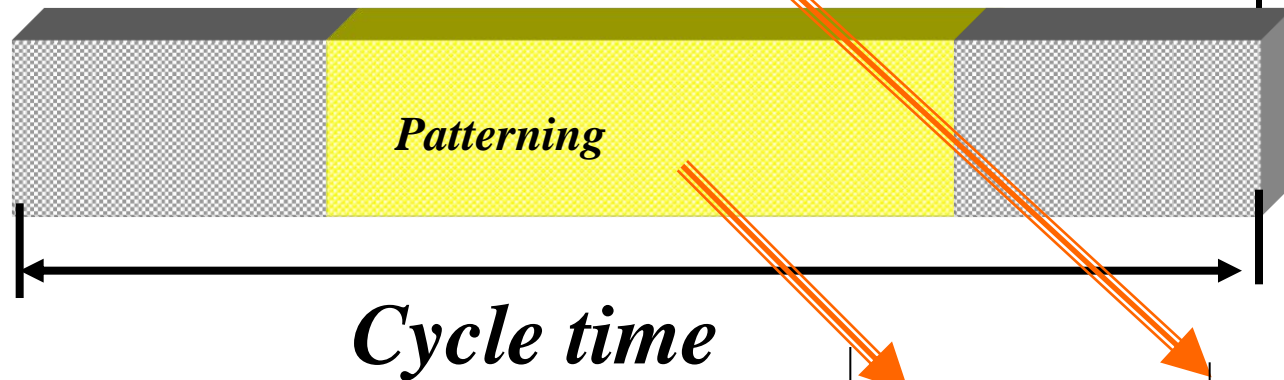


Cycle time can not be described on CoO

■ Single Exposure

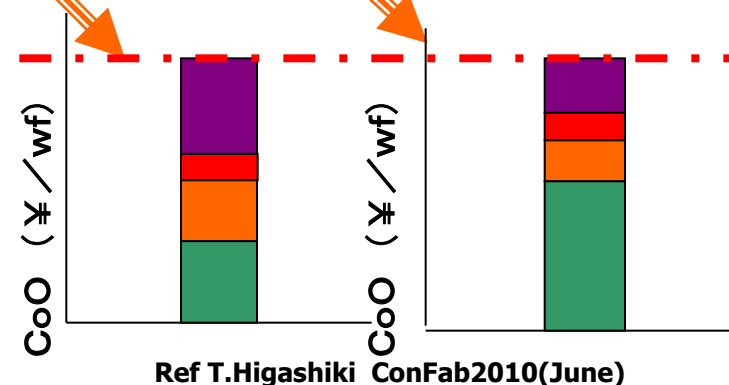


■ DPT



DPT Economical Problems

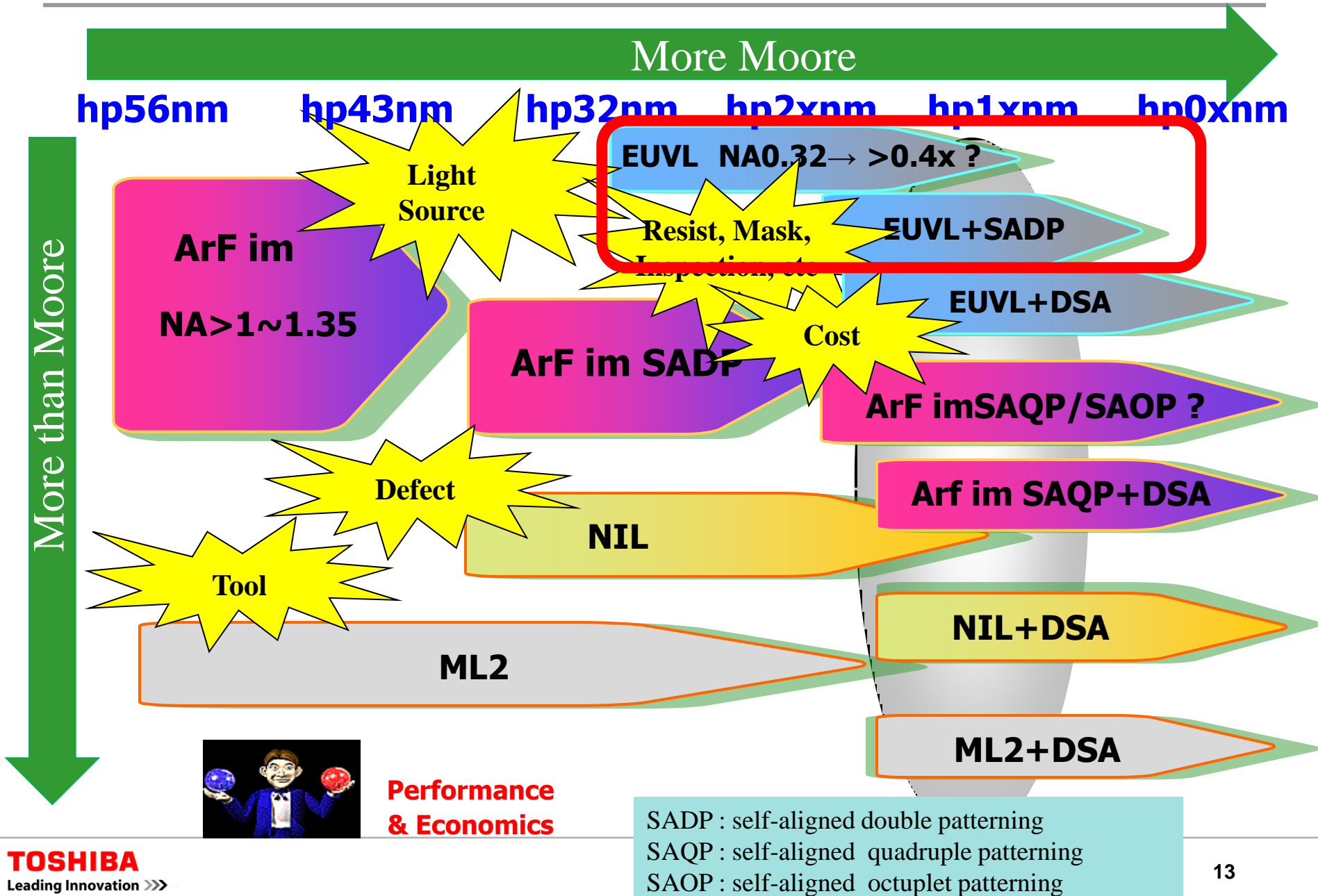
- ✓ Investment Cost (LP, Etching , M&I, etc.)
- ✓ Mask Cost
- ✓ Opportunity Cost (“Time is money”)



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Lithography Challenges



EUVL Challenges for NAND Memory

Mask Defect Control DD<0.1/cm²

✓ Inspection

- **ABI (Actinic Blanks Inspection)**
- **PI (Pattern Inspection)**
- **Inspection after Pattern Repairing**

Resist Performance

**Resolution < 16nm, LWR < 2nm, Photo
Speed < 20mj/cm², Defectivity < 0.1/cm²**

Light Source Performance

**Enough Power for Throughput > 150wph
Operational Cost (Mirror, E Power, DMT, etc)**



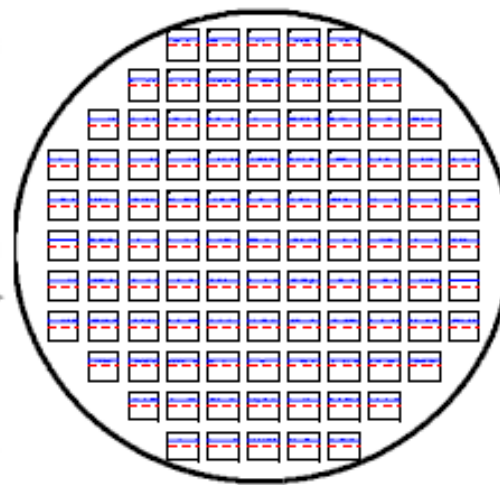
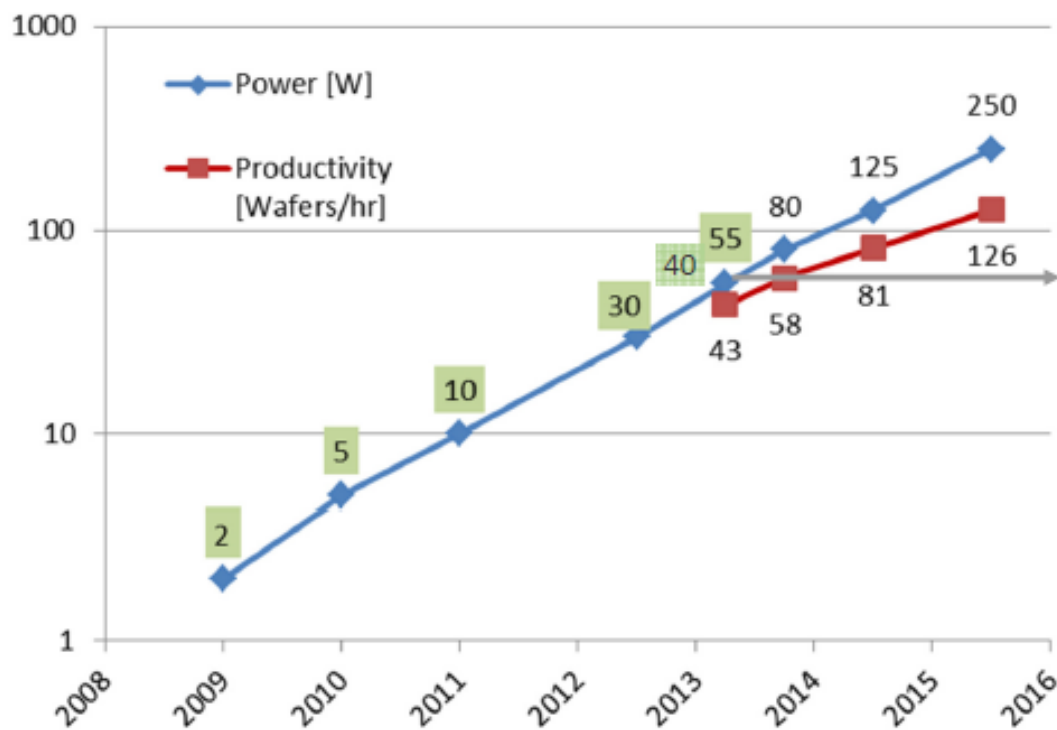
EUV Source Power Progress reaching 55 W

Supporting 43 Wafers/hr, 250 W target to be reached in 2015

ASML

Public

Slide 38



At 55 W, 1 run:
97.5% of the dies < 0.5% dose

At 40 W, 6 runs:
99.99 of the dies < 0.2% dose,

7 one hour runs total representing
~ 250 exposed wafers @ 15 mJ/cm²

EUV Collaboration

TOSHIBA

Device
&
design

Lithography

- Pattern Layout Tech. (OPC/DFM)
- Specification Design for Tools
- Mask process
- Resist process

Si
Process



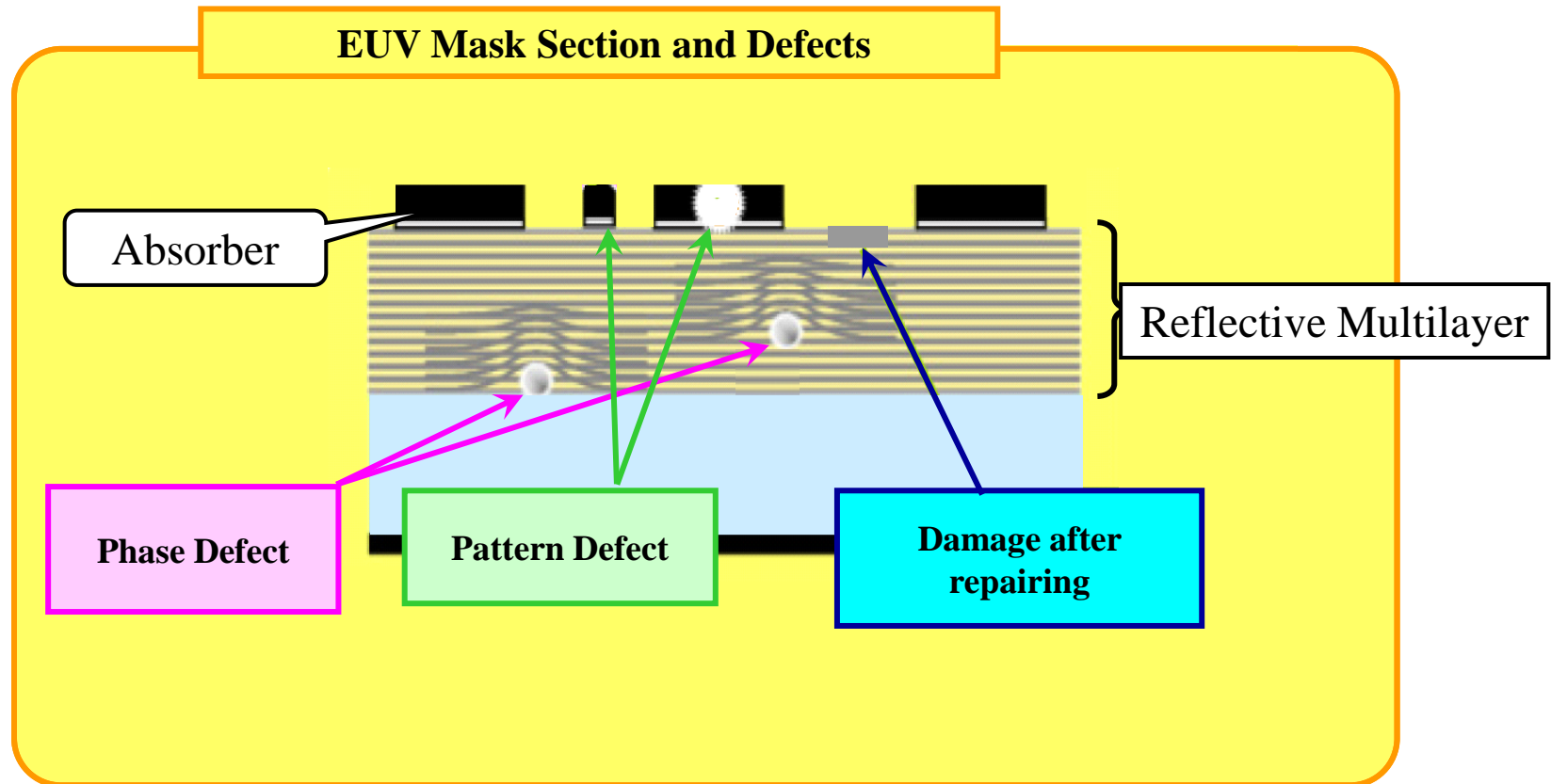
Advanced EUVL

Mask Quality
Mask Inspections
Resist Quality
High NA Exposure
EUVL+DSA

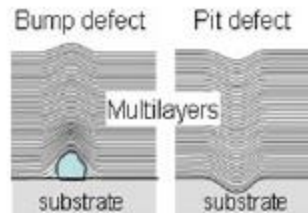
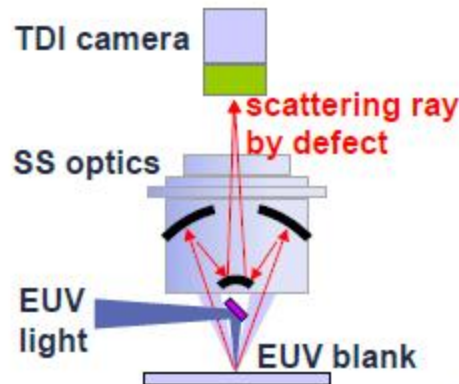
Suppliers

Exposure Tool EDA
Resist Material Mask
Metrology and Inspection

Structure of EUVL Mask



ABI Chronicle



POC by MIRAI I,II (2001-2005)
feasibility of ABI,
dark field ABI by AIST



Proto by MIRAI-Selete(2006-2010)
full mask area ABI inspection



HVM by EIDEC(2011-)
ABI for hp16nm HVM
w/ Lasertec

-Development target-
1nmH/50nmW detection
in 45 min. scan

ABI coherent development strategy

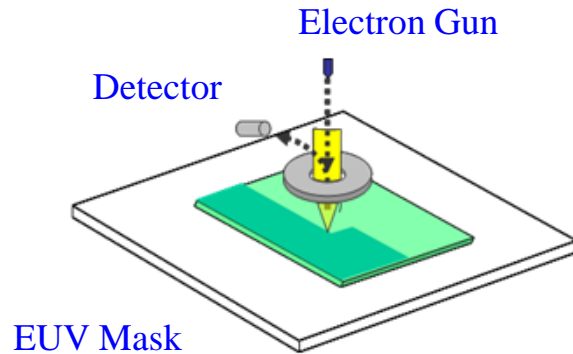


EIDEC Symposium 2013 May 21, 2013

5

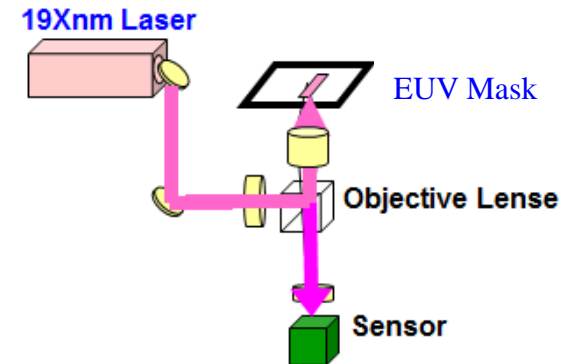
EB inspection tool

**Sensitivity :
Similar to SEM**



Detector: TDI Sensor

**Throughput :
Similar to Optical**



EBeyeM

Electron Gun

Continuous
Moving (Y)

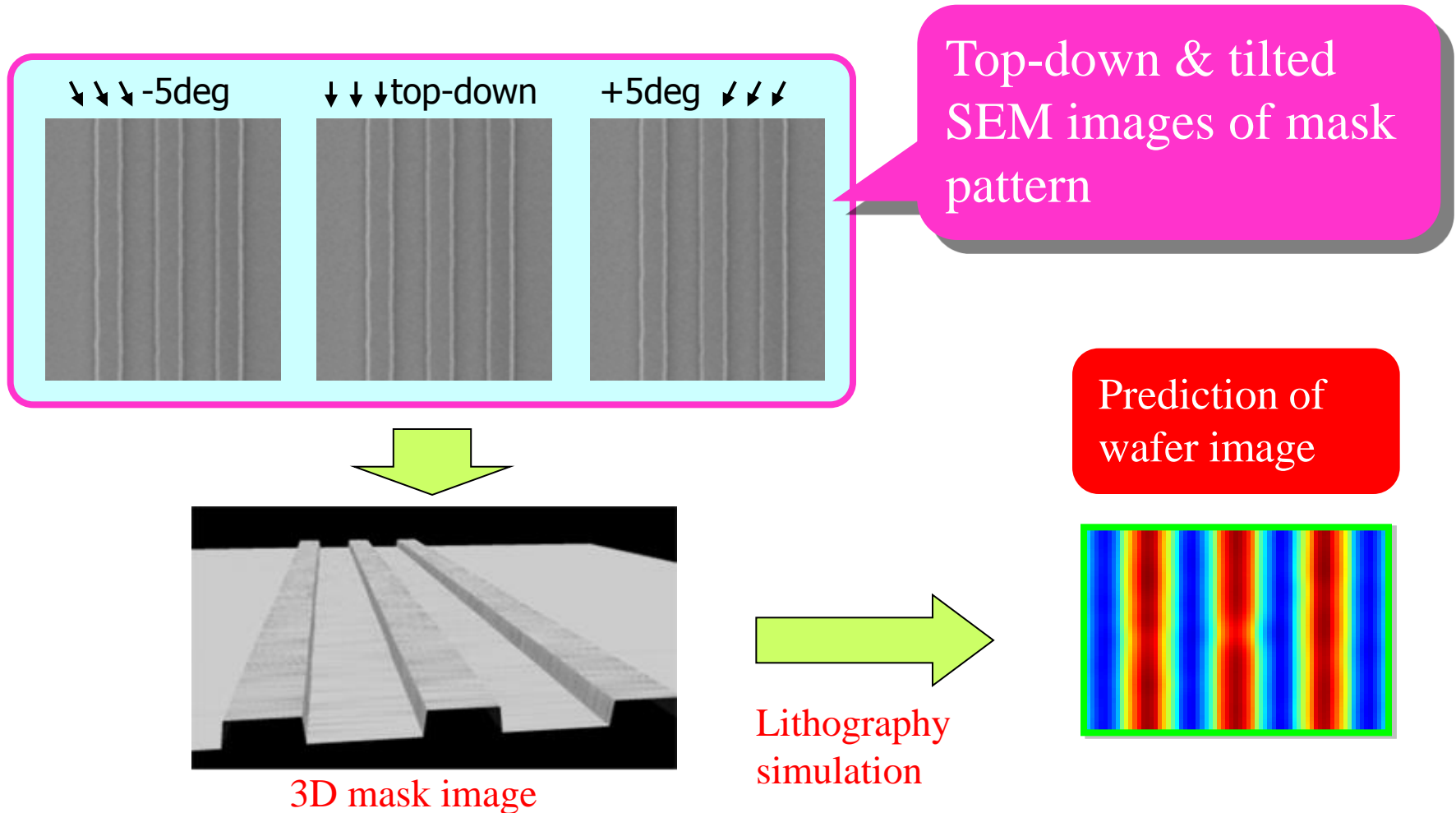
Stepping (X)

**Projection Electron
Microscope**

EUV Mask

Quality assurance of hotspot & repaired pattern

- EUV AIMS operation will be difficult in 2012.
- 3D SEM + Litho. Simulation will be applied.



Toshiba Technology Scenario for EUV Mask

	HP 2Xnm	HP 1Xnm
Multilayer defect inspection	DUV inspection	Actinic inspection
Patterned mask inspection	DUV inspection	EB inspection
Defect repair	EB repair	
Hotspot & repaired pattern assurance	Litho. Sim. w/ 3D mask image	EUV-AIMS
Particle inspection	EB inspection	



ready

under developing

Absorber Pattern Generation

EB writer : "EBM8000"

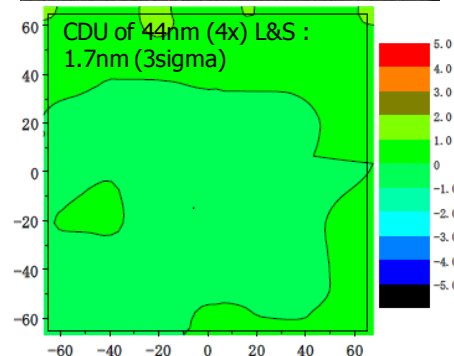
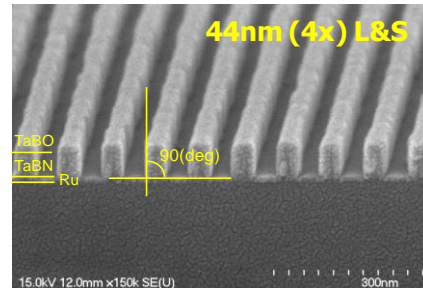
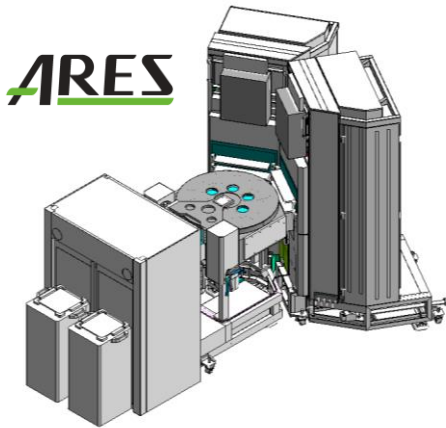
(NuFlare)



<http://www.nuflare.co.jp/product/ebm.html>

Dry Etching Equipment : "ARES_{TM}"

(Shibaura Mechatronics)



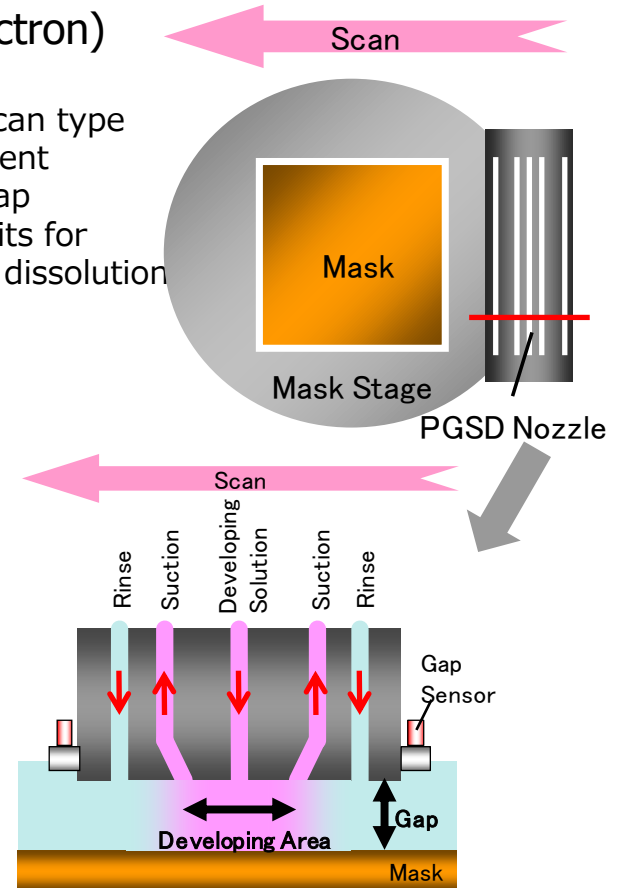
Iino, et al. (BACUS2010)

Etched absorber pattern has capability for scaling down to hp1x EUVL single exposure.

Scanning-type Developer : "PGSD" Proximity-Gap-Suction-Development System

(Tokyo Electron)

- ❑ Slit and scan type development
- ❑ Narrow gap
- ❑ Suction slits for removing dissolution products



Cross-sectional view

- ✓ Extreme high uniformity of developing solution supply
- ✓ Nearly zero loading effect caused by dissolution products

“SMRAT Network of Mask & Lithography”

Toshiba R&D Center

DTF

- Mask House

NUFLARE

- EB Writer
- Inspection

SHIBaura

- Cleaning Tech.
- Etching



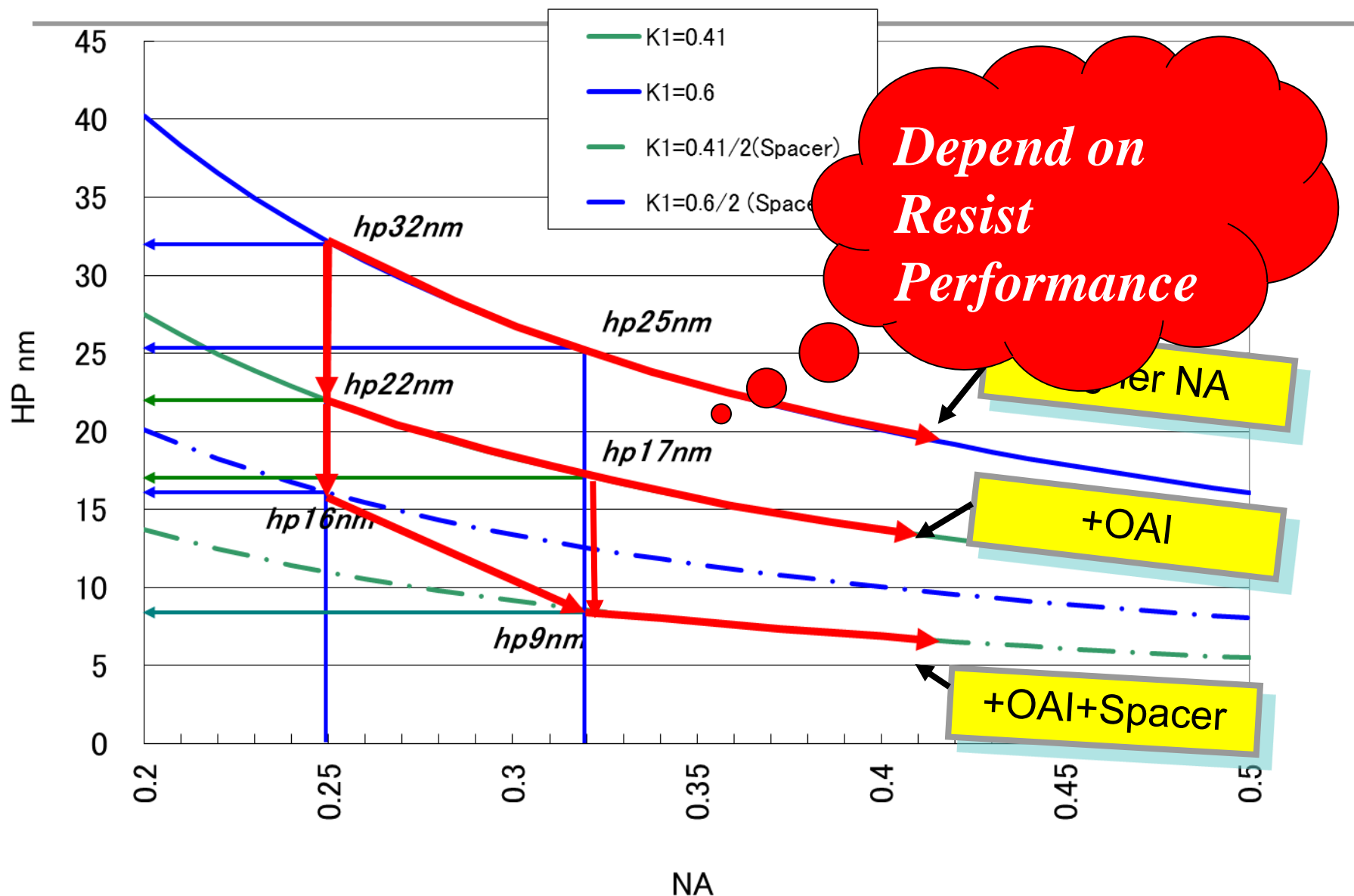
(EUVL Infrastructure
Development Center)

- Mask Inspections
- High Performance Resist
- Sub-10nm DSA material

Toshiba Advanced Litho.& Mask Dept.

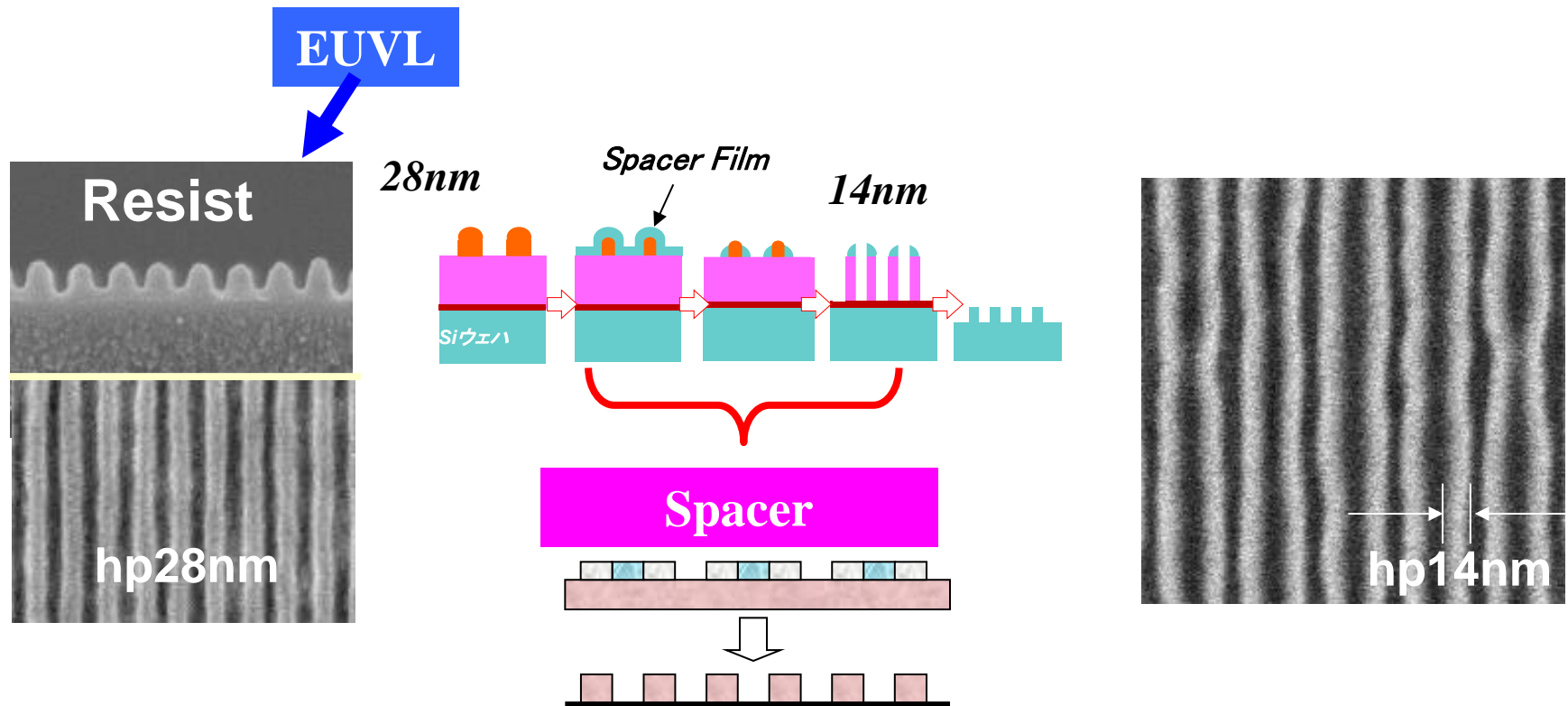
- Advance Mask & Litho
- Computational Litho
- OPC/DFM
- Next Emerging Litho.

Resolution Limit of EUVL



EUVL and SADP Complementally

hp14nm Exposure was Realized by EUVL + SADP

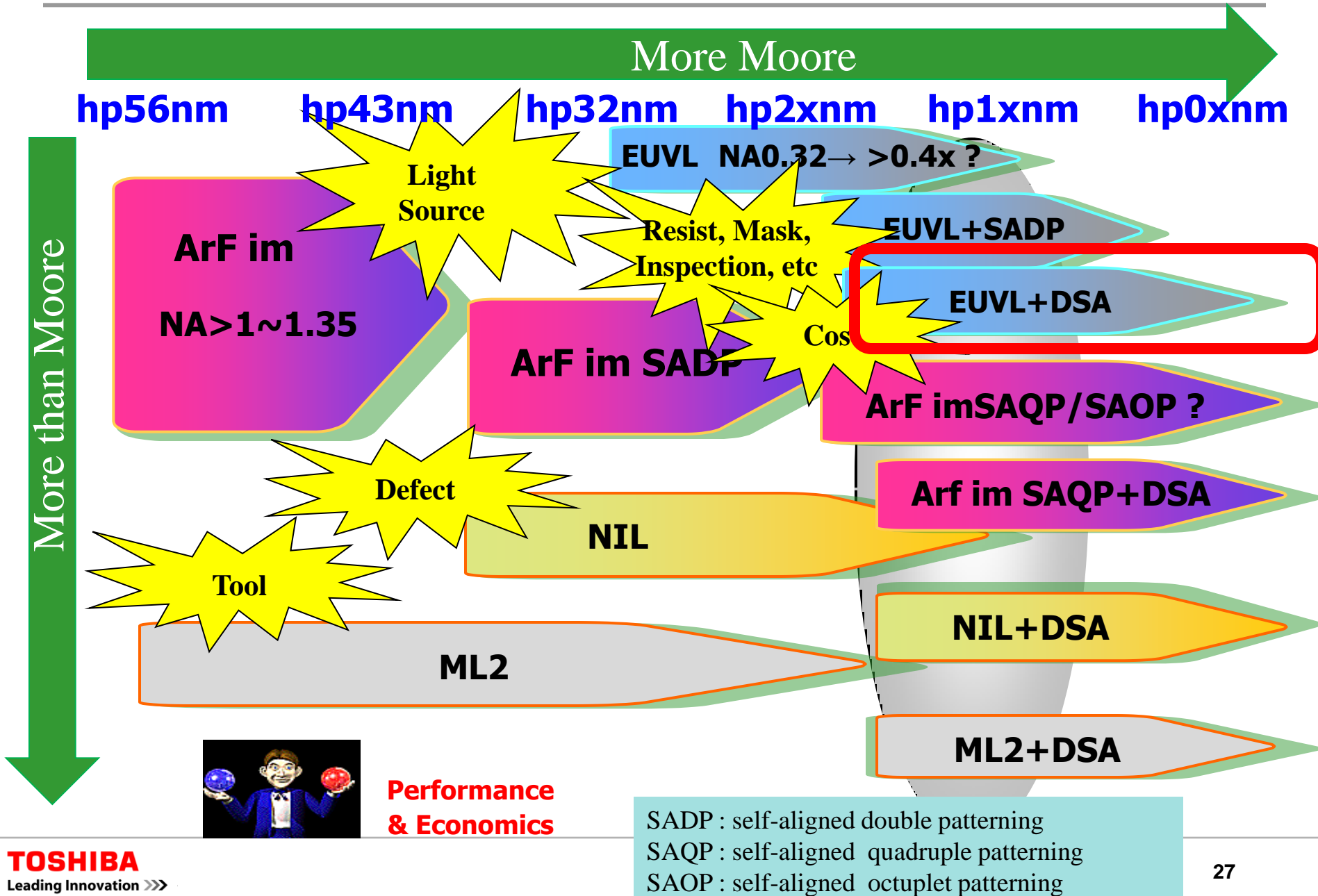


Y. Watanabe et al, Photomask Japan 2010(April)

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Si
Process



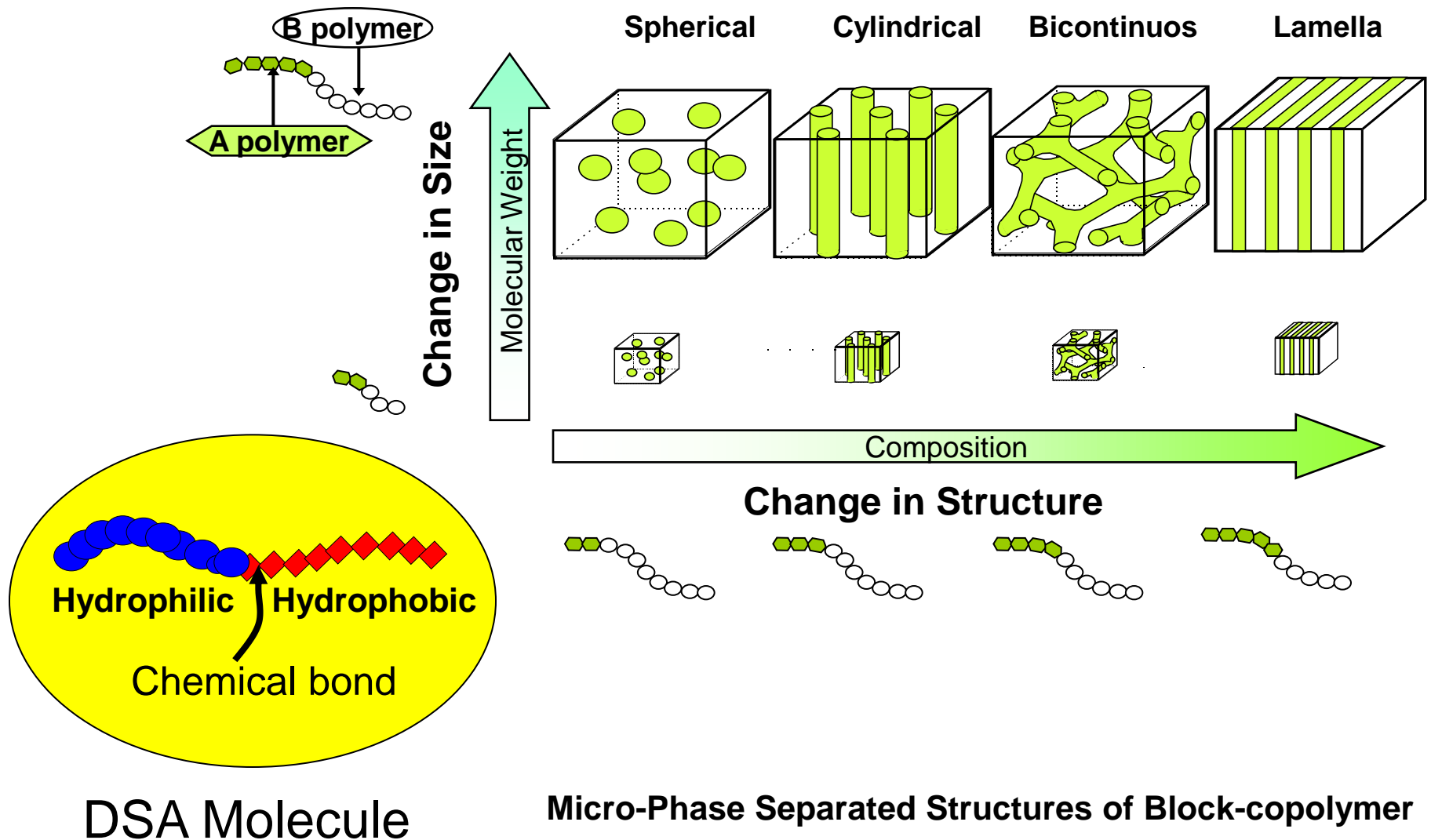
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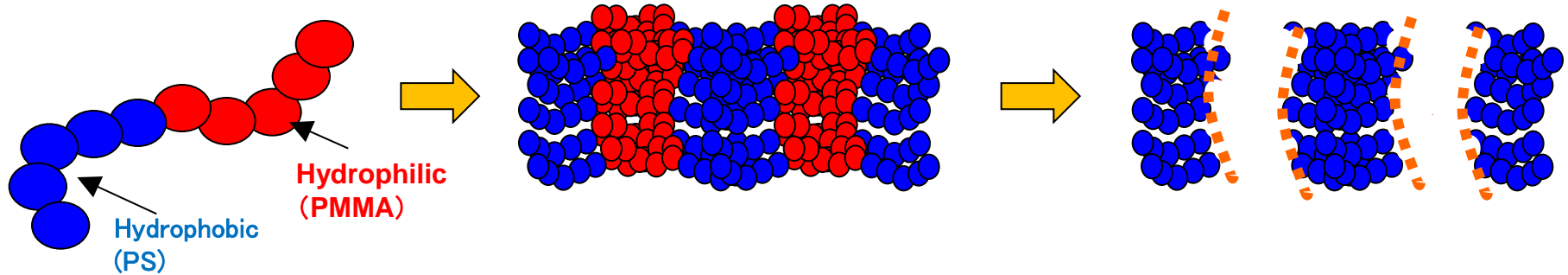
Suppliers

Exposure Tool EDA
Resist Material Mask
Metrology and Inspection

DSA (Directed Self Assembly)

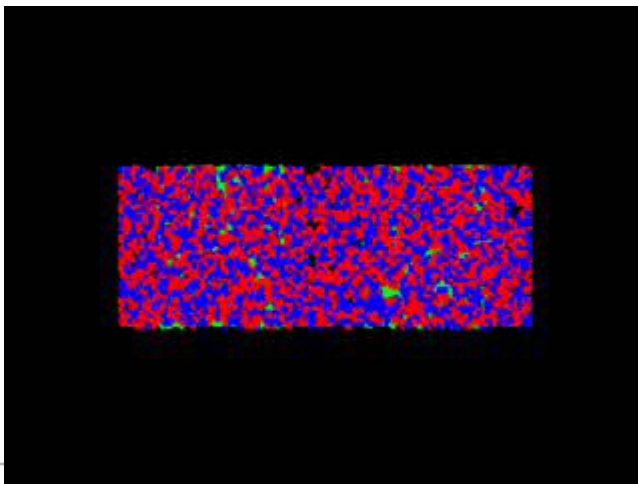


DSA (Directed Self Assembly)

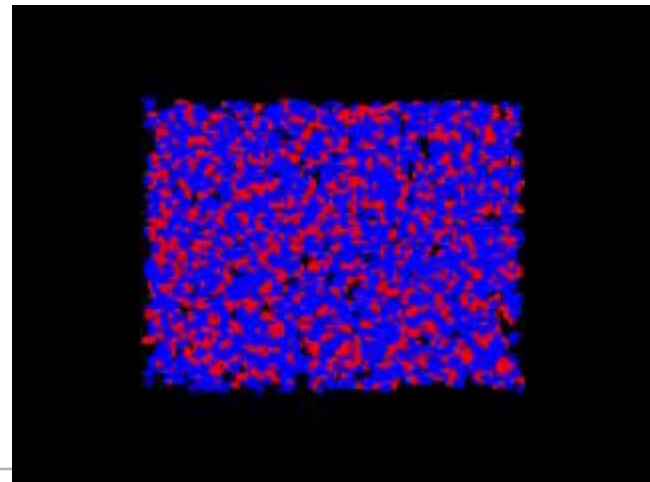


BCP: Block copolymer

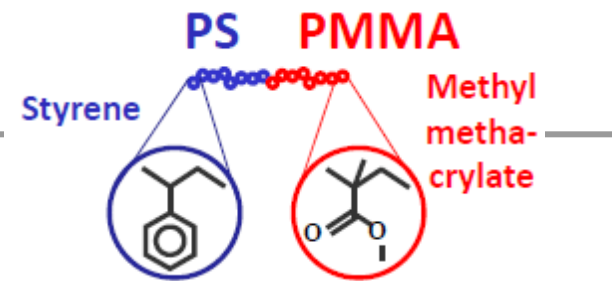
Line & Space



Contact Hole

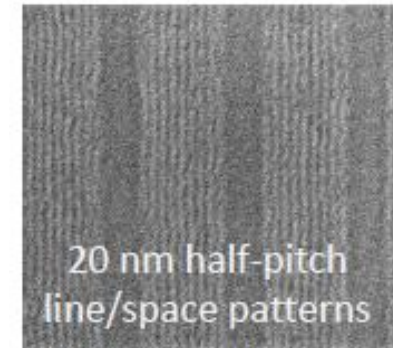
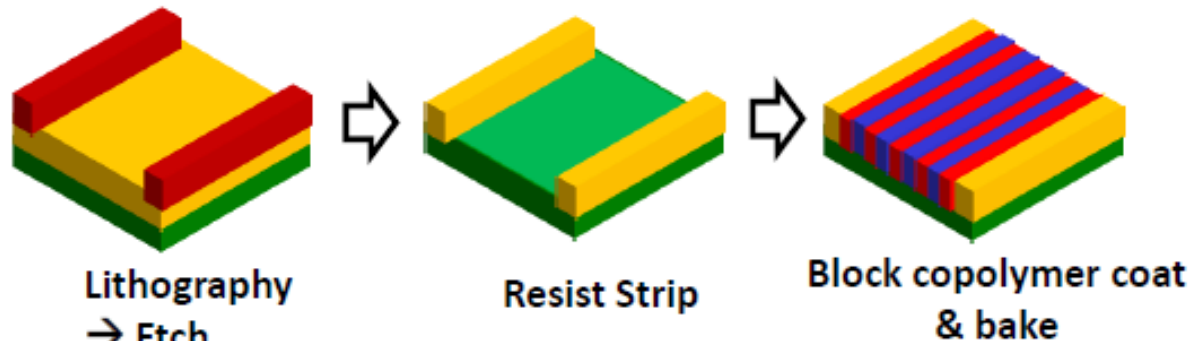


Grapho-Epitaxy & Chemo-Epitaxy



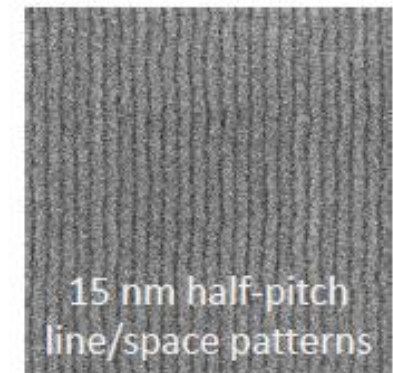
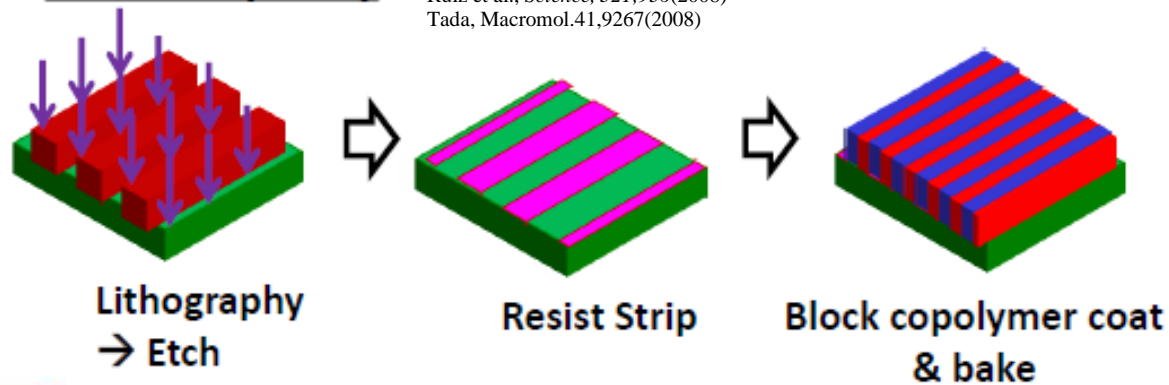
Grapho-Epitaxy

Segalman et al., *Adv.Mater.* 3,1152(2001)
Nato et al., *IEEE Trans. Magn.* 38,1949(2002)
Chen et al., *Appl.Phys.Lett.* 81,3657(2002)



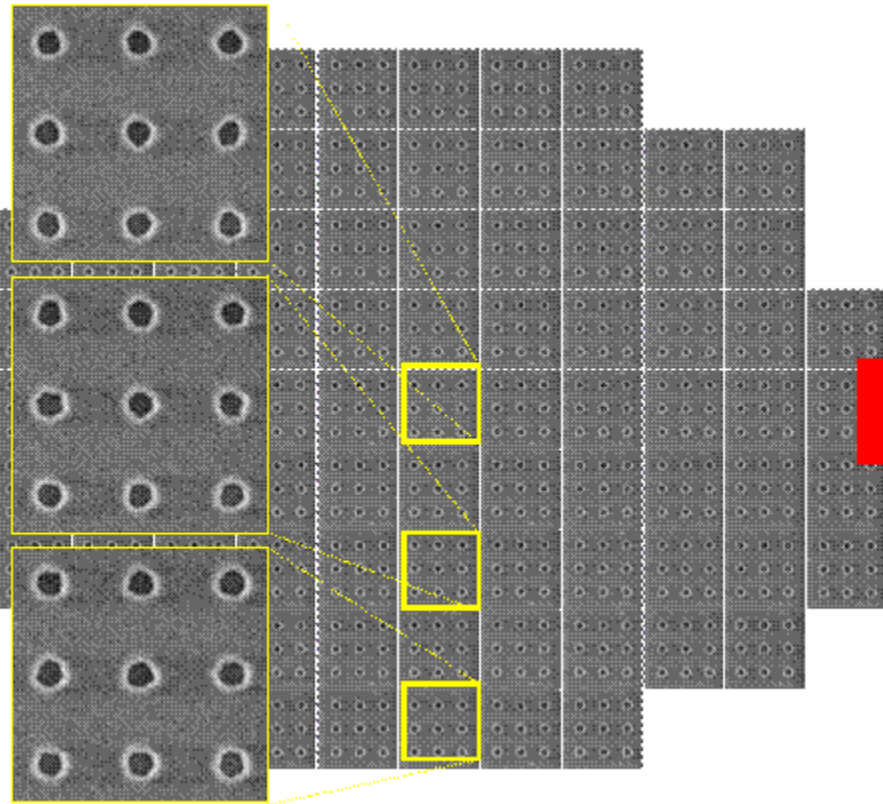
Chemo-Epitaxy

Chen et al., *Adv.Mater.* 20,3155(2008)
Rulz et al., *Science*, 321,936(2008)
Tada, *Macromol.* 41,9267(2008)



Guide Hole vs. DSA Hole

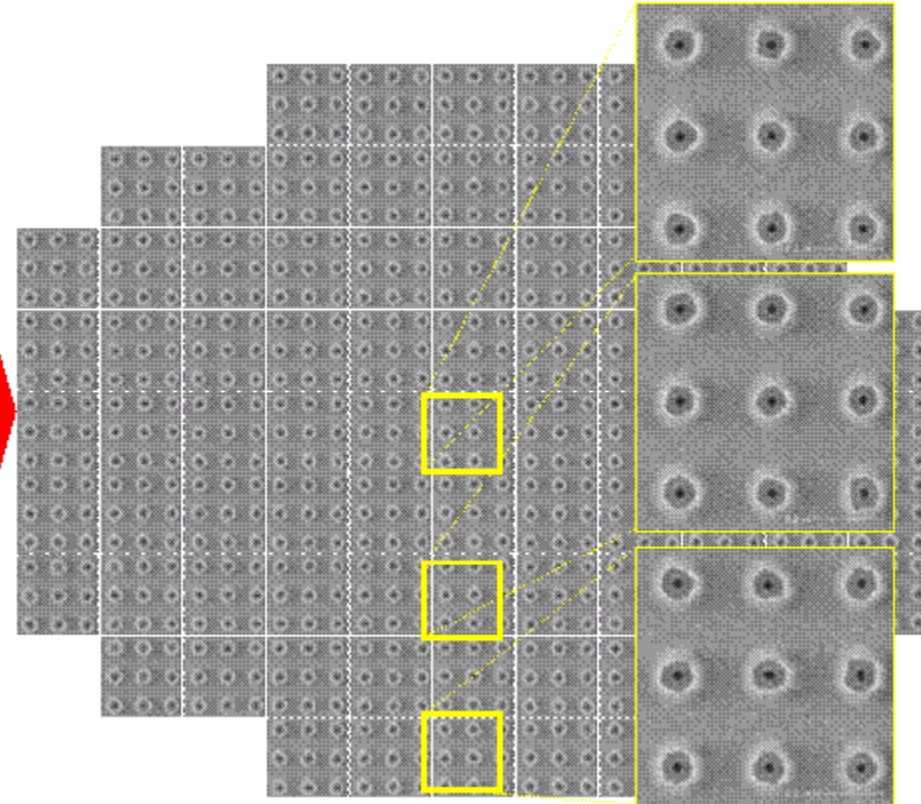
Guide hole



Ave. CD	72.1nm
---------	--------

3sigma	7.6nm
--------	-------

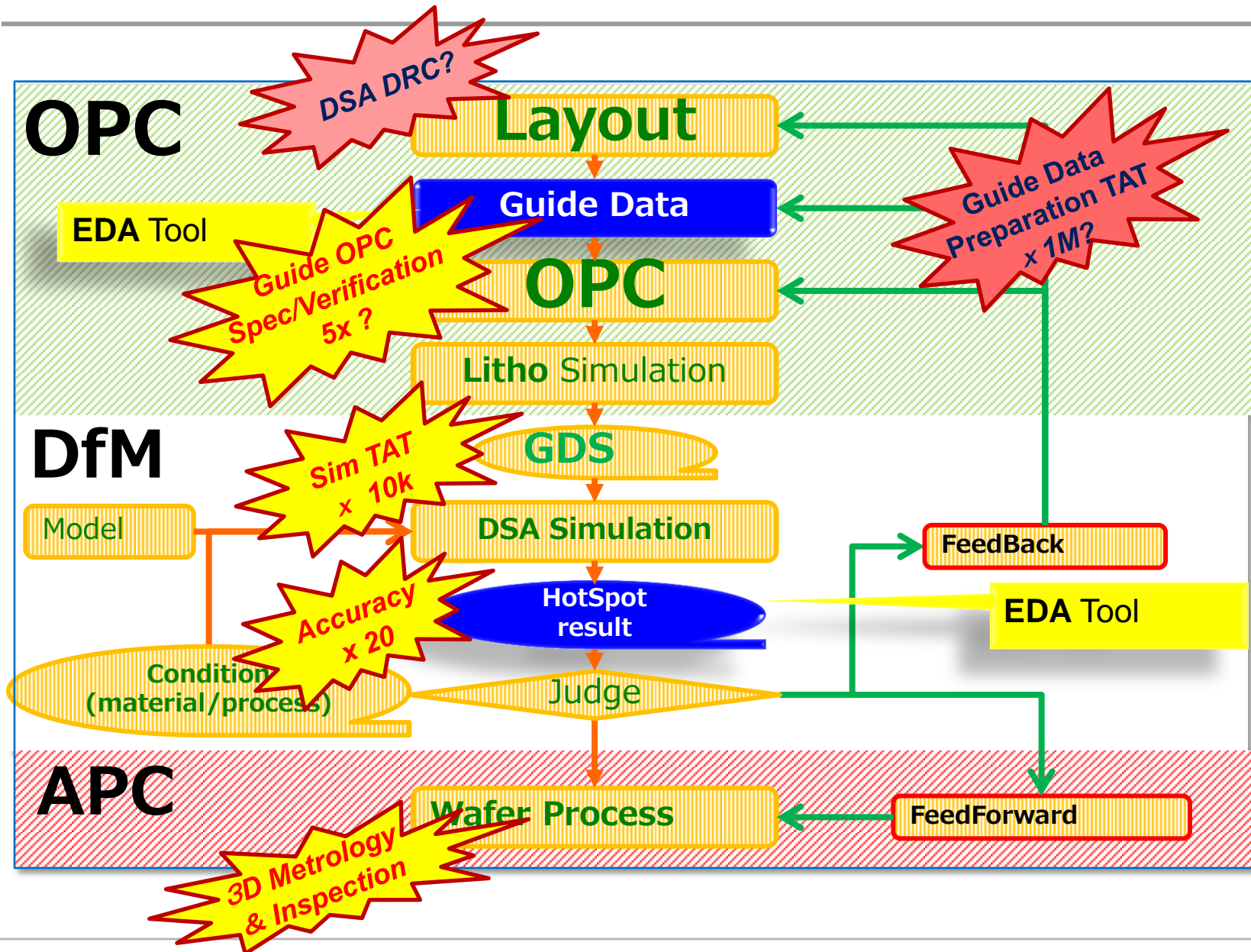
DSA hole



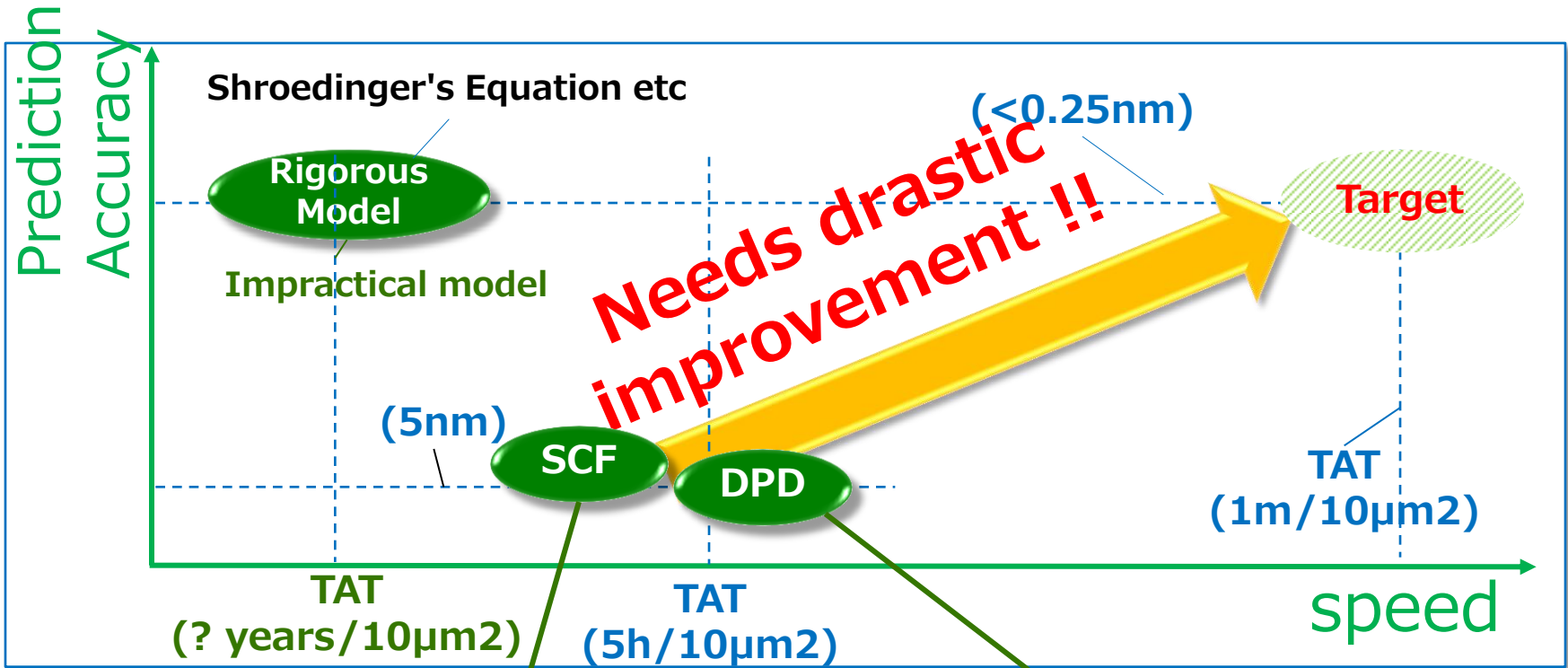
Ave. CD	28.5nm
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3sigma	1.3nm
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DSA OPC/DfM/APC Flow



DSA Simulation Model

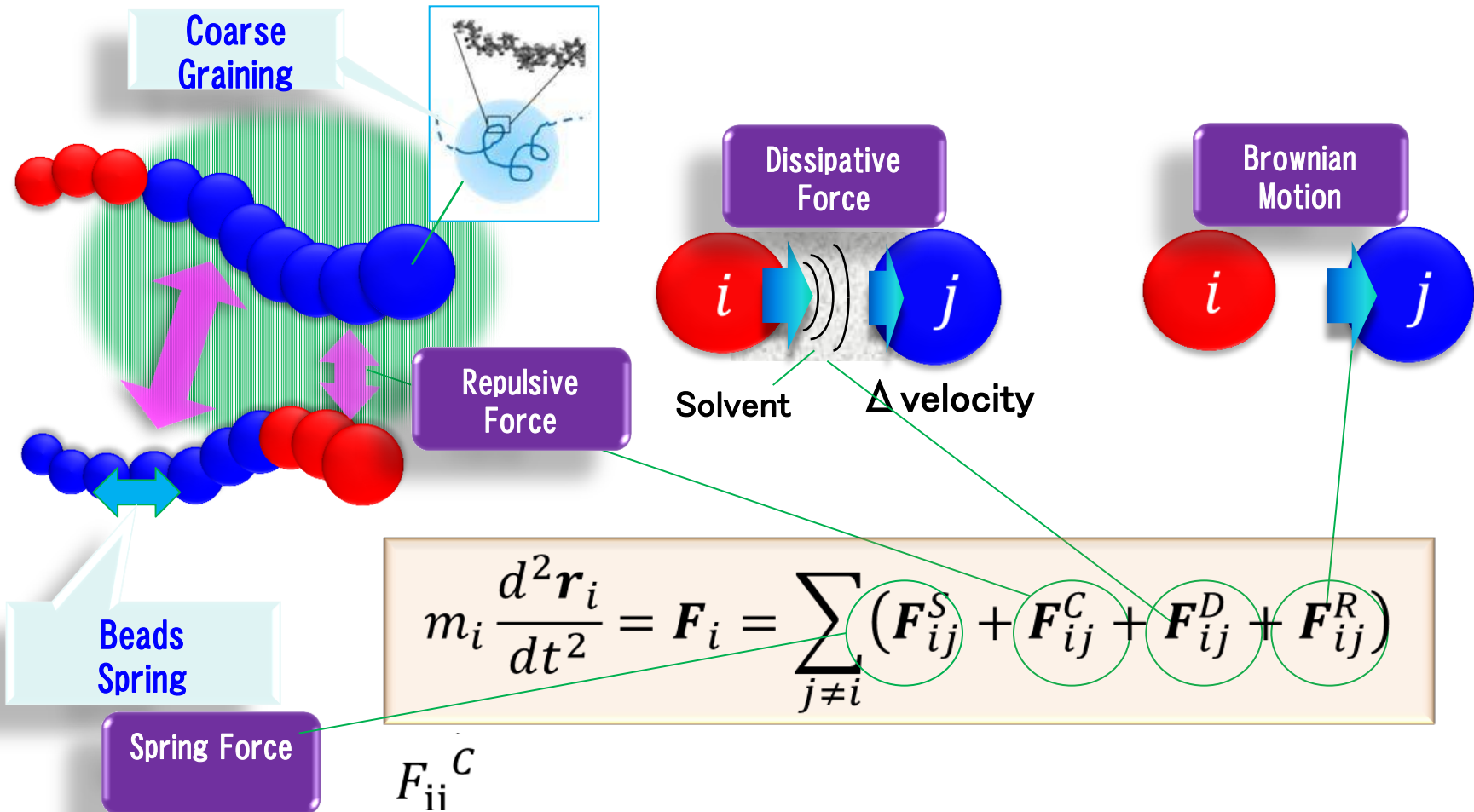


Model	Self Consistent mean Field	Dissipative Particle Dynamics
methodology	Based on statistical field theory	Based on Newton's motion equation
Challenge	Modeling of thermal fluctuations	Difficult to fit to a measured data

DSA Simulation Model

◆ Molecular Dynamics based Coarse Grained MD DPD (Dissipative Particle Dynamics)

Available Free Software Tools are;
LAMMPS /GROMAX/ OCTA-COGNAC,,



Challenges for DSA Lithography

- **High performance DSA material**
 - High χ material
 - Resolution, LWR/LER, Etching
- **Long term stability**
 - Robust material and tool for environmental control such as surface energy stability, temperature, humidity, pressure and PH, etc.
 - Defectivity, CD and overlay accuracy
- **Development of molecular dynamics based DSA simulator**
 - More accurate simulation model
 - BCP and related molecular design
 - Microphase separation (2D/3D)
 - TAT / accuracy trade-off
- **DSA OPC/DFM technology**
 - Design rule verification
 - DSA and guide patterning (litho/wet/dry)
- **Metrology & Inspection**
 - Metrology for 3D profile
 - Inspection technology for 1xnmhp and beyond needs to overcome throughput / accuracy / sensitivity trade-off.

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Conclusion

- **Economical factor is dominant criteria for a lithography strategy**
 - ✓ **For Memory Device; Throughput, Investment & Si Process Cost**
 - ✓ **For Logic Device ; Mask Cost, Cycle Time**

- **EUVL**
 - ✓ **Moving from R&D phase to production**
 - ✓ **Light source performance is improving, but a significant concern.**

- **DSA**
 - ✓ **DSA will be a complementary technology for all other lithography**
 - ✓ **EUVL+DSA will be one of candidates for sub 10nm lithography.**

- ◆ **Next Challenges**
 - ✓ **Next generation lithography will depend on innovation of infrastructure technologies such as OPC, DFM, M&I, etching and cleaning.**

TOSHIBA

Leading Innovation >>>

